R18

Code No: 153AG

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech II Year I Semester Examinations, February - 2024

COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to CSE, CSBS, CSIT, CE(SE), CSE(CS), CSE(DS), CSE(N), AI&DS, AI&ML, CSD)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	What is the purpose of control unit?	[2]
b)	Illustrate logical right shift operation.	[3]
c)	What is the use of micro program sequencer?	[2]
d)	List data transfer instructions.	[3]
e)	Give 2'complement representation of -12.	[2]
f)	How to store English alphabet in binary?	[3]
g)	What is asynchronous transfer?	[2]
h)	What is associate memory?	[3]
i)	What is an array processor?	[2]
j)	State cache coherence problem.	[3]

PART – B

(50 Marks)

2.a)	Discuss the problems to be faced by a computer designer.	
b)	Differentiate between computer organization and computer architecture.	[5+5]

OR

3.	Explain the construction of a bus system for four registers with necessary circuit diagram.	[10]
4.a)	Make a comparison of hardwired control with micro programmed control.	
b)	Discuss about instruction formats.	[5+5]

OR

5.	With suitable instruction explain various addressing modes used in today's computers.	[10]
6.	With the help of a flowchart demonstrate multiplication of two floating point numbers.	[10]

OR

7.	Discuss decimal addition operation on two numbers with necessary circuit diagram.	[10]

8. Design a parallel priority interrupt hardware for a system with eight interrupt sources and explain your design. [10]

OR

9. Discuss organization of a 2M × 32 memory module using 512K × 8 static memory chips with a diagram. [10]

10. Explain the arithmetic pipeline for floating point addition and subtraction with help of flowchart. [10]

OR

11. What is an interchange switch? Explain the operation of a 2 × 2 interchange switch. [10]

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